This listing of claims will replace all prior versions and listings of the claims in the application:

1. (Original) A method of forming a nonvolatile memory device, comprising:

forming a first oxide layer on a substrate;

forming a nitride layer on the first oxide layer;

forming a second oxide layer on the nitride layer;

patterning the second oxide layer so as to expose the nitride layer;

forming a first polysilicon layer on the second oxide layer and the exposed portion of the nitride layer;

etching the first polysilicon layer and the nitride layer so as to expose the second oxide layer and the first oxide layer and to form polysilicon spacers on the nitride layer;

etching the polysilicon spacers so as to expose portions of the nitride layer, the exposed portions of the nitride layer comprising charge trapping layers;

etching the exposed portion of the first oxide layer to expose a portion of the substrate;

forming a third oxide layer on the exposed portion of the substrate, the exposed portions of the nitride layer, and the second oxide layer;

forming a second polysilicon layer on the third oxide layer; and

planarizing the second polysilicon layer so as to expose the second oxide layer, the second polysilicon layer comprising a gate electrode that overlaps portions of the charge trapping layers, the third oxide layer comprising a gate insulating layer.

2. (Original) The method of Claim 1, further comprising:

etching the exposed portion of the second oxide layer, the nitride layer, and the first oxide layer using the gate electrode as a mask so as to expose the substrate.

3. (Original) The method of Claim 2, further comprising:

forming a source region and a drain region in exposed portions of the substrate on adjacent sides of the gate electrode.

4. (Original) The method of Claim 3, wherein forming the source region and the drain region comprises:

forming the source region and the drain region in exposed portions of the substrate on adjacent sides of the gate electrode using ion implantation.

5. (Canceled)

6. (Canceled)

7. (Original) The method of Claim 1, wherein forming the first oxide layer on the substrate comprises:

forming the first oxide layer on the substrate using thermal oxidation.

8. (Original) The method of Claim 1, wherein forming the nitride layer on the first oxide layer comprises:

forming the nitride layer using low-pressure chemical vapor deposition on the first oxide layer.

9. (Original) The method of Claim 1, wherein forming the second oxide layer on the nitride layer comprises:

forming the second oxide layer using low-pressure chemical vapor deposition on the nitride layer.

10. (Original) The method of Claim 1, wherein etching the first polysilicon layer comprises:

etching the first polysilicon layer using an isotropic etch back process.

11. (Original) The method of Claim 1, wherein etching the exposed portion of the first oxide layer comprises:

etching the exposed portion of the first oxide layer using a wet etching process.

12. (Original) The method of Claim 1, wherein forming the third oxide layer on the exposed portion of the substrate, the exposed portions of the nitride layer, and the second oxide layer comprises:

forming the third oxide layer on the exposed portion of the substrate, the exposed portions of the nitride layer, and the second oxide layer using chemical vapor deposition.

13. (Original) The method of Claim 1, wherein forming the second polysilicon layer on the third oxide layer comprises:

forming the second polysilicon layer on the third oxide layer using chemical vapor deposition.

14. (Original) The method of Claim 1, wherein planarizing the second polysilicon layer comprises:

planarizing the second polysilicon layer using chemical mechanical polishing.

15 - 31. (Canceled)

32. (Original) A method of forming a non-volatile memory device, comprising:

forming a first oxide layer on a substrate;

forming a nitride layer on the first oxide layer;

forming a second oxide layer on the nitride layer wherein a portion of the nitride layer is exposed between portions of the second oxide layer;

forming spacers on exposed portions of the nitride layer adjacent the second oxide layer so that a portion of the nitride layer remains exposed between the spacers;

removing portions of the nitride layer and the first oxide layer exposed by the spacers to thereby expose portions of the substrate between the spacers;

removing the spacers;

forming a third oxide layer on the exposed portion of the substrate, on exposed portions of the nitride layer adjacent the second oxide layer, and on the second oxide layer;

forming a conductive electrode on the third oxide layer between the portions of the second oxide layer.

33. (Original) A method according to Claim 32 wherein forming the conductive electrode comprises:

forming a conductive layer on the third oxide layer between portions of the second oxide layer and opposite the second oxide layer; and

planarizing the conductive layer to expose oxide of the second oxide layer and/or third oxide layer.

34. (Original) A method according to Claim 33, further comprising:

after planarizing the conductive electrode, removing remaining portions of the third oxide layer, the second oxide layer, the nitride layer, and the first oxide layer exposed by the planarized conductive electrode.